SUMMiT V™
Five Level Surface Micromachining Technology
Design Manual

Version 1.2 – 11/01/2001
MEMS and Novel Silicon
Science and Technology Department
Microelectronics Development Laboratory
Sandia National Laboratories
PO Box 5800, Albuquerque, NM 87185

Before starting SUMMiT V™ Design, Contact Department 1769, or email: drt@sandia.gov to ensure you have the latest release of the Design Manual. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-AC04-94AL85000

I: Overview and Technology Description

SUMMiT V™ (Sandia Ultra-planar Multi-level MEMS Technology V) is a 1.0 micron, 5-level, surface micromachining (SMM) technology featuring four mechanical layers of polysilicon fabricated above a thin highly doped polysilicon electrical interconnect and ground plane layer. Sacrificial oxide is sandwiched between each polysilicon level. The thin sacrificial film defines the amount of mechanical play in gear hubs and hinges. The oxide directly beneath the upper two levels of mechanical polysilicon are planarized using a chemical mechanical polishing (CMP) process, which alleviates several photolithographic and film etch issues while freeing the designer from constraints that would otherwise be imposed by the underlying topography

The entire stack, shown below in Figure 1, is fabricated on a 6-inch single crystal silicon wafer with a dielectric foundation of 0.63 µm of oxide and 0.80 µm of nitride.

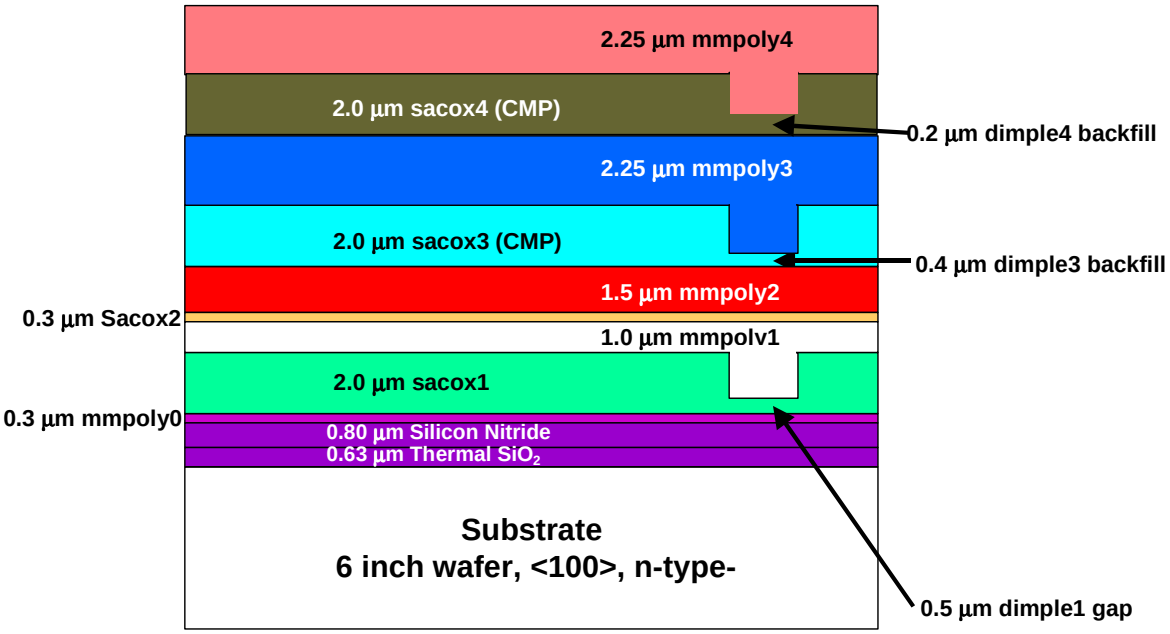


Figure 1. Drawing of the SUMMiT V™ structural and sacrificial layers

The layers of polysilicon are designated from the substrate up as MMPOLY0 through MMPOLY4. Prefixing these levels with “MM” for micromechanical prevents confusion with layer names often used in CMOS processes. The sacrificial films are designated as SACOX1 through SACOX4, with the numerical suffix corresponding to the number of the subsequent layer of mechanical polysilicon that is deposited on a given oxide.

The cross section in Figure 2 represents the various types of features that can be created from the 14 individual masks defined in Table 1 and the SUMMiT V™ fabrication sequence.

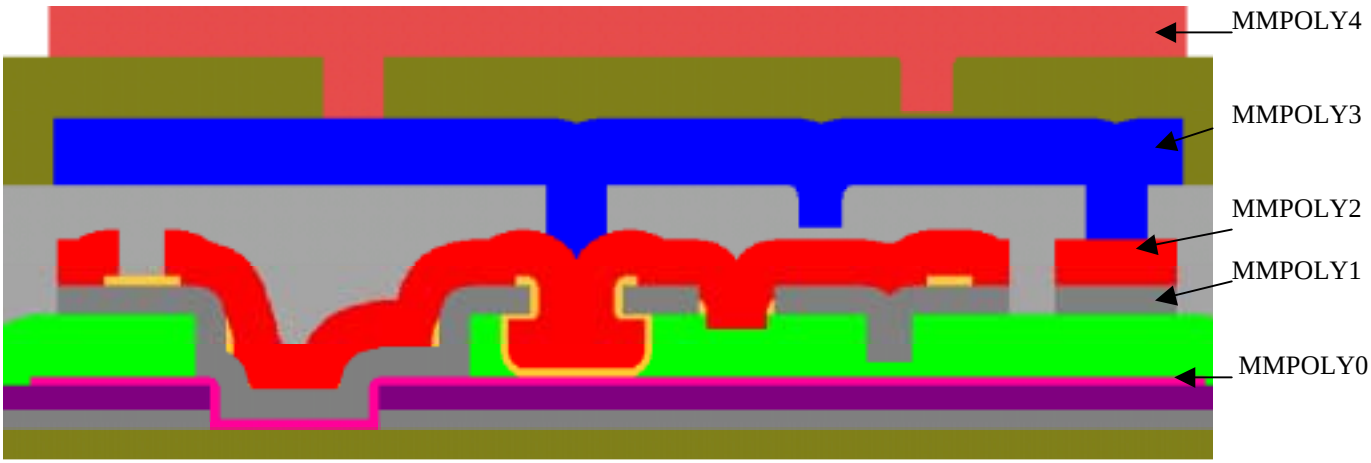


Figure 2. Cross-section of SUMMiT V stack showing features realizable through the fabrication process.

Table 1 : SUMMiT V™ MASKING LAYERS

MASK NAME	MASK LEVEL	FIELD	ALIGNS TO LEVEL*	PRIMARY PURPOSE	LAYER NUMBER (GDSII)
NITRIDE_CUT (NIC)	1	Dark	N/A	Substrate contacts	21
MMPOLY0 (P0)	2	Clear	NITRIDE_CUT	Ground plane and electrical interconnects	22
DIMPLE1_CUT (D1C)	3	Dark	MMPOLY0	Dimples in MMPOLY1	23
SACOX1_CUT (X1C)	4	Dark	MMPOLY0	Anchor for MMPOLY1	24
PIN_JOINT_CUT (PJC)	5	Dark	MMPOLY0	Cut in MMPOLY1 with constraint flange	26
MMPOLY1_CUT (P1C)	6	Dark	MMPOLY0	Cut in MMPOLY1 without constraint flange	25
SACOX2 (X2)	7	Clear	MMPOLY0	Defines hub/hinge play	27
M1MPOLY2 (P2)	8	Clear	MMPOLY0	Patterns MMPOLY2 and/or MMPOLY1 + MMPOLY2	28
DIMPLE3_CUT (D3C)	9	Dark	MMPOLY0	DIMPLEs in MMPOLY3	29
SACOX3_CUT (X3C)	10	Dark	MMPOLY0	Anchor MMPOLY3	30
MMPOLY3 (P3)	11	Clear	SACOX3_CUT	Patterns MMPOLY3	31
DIMPLE4_CUT (D4C)	12	Dark	MMPOLY0	DIMPLEs in MMPOLY4	34
SACOX4_CUT (X4C)	13	Dark	MMPOLY0	Anchor MMPOLY4	42
MMPOLY4 (P4)	14	Clear	SACOX4_CUT	Patterns MMPOLY4	36

* Alignment tolerance to reference layer is better than 0.5μm.

Drawing Only Layers

In addition to the layers shown in Table 1, five have been created to facilitate layout and are referred to as "drawing only" layers. Listed in Table 2, these layers do not directly define a mask, but are instead XORed with their corresponding master layer to define the mask used during the fabrication process.

Table 2: SUMMiT V™ DRAWING ONLY LAYERS

LAYER NAME	XORed WITH LAYER	PRIMARY PURPOSE
MMPOLY1 (P1)	P1C	Define MMPOLY1 within a MMPOLY1_CUT boundary
SACOX2_CUT (X2C)	X2	Define holes/openings within a SACOX2 boundary
MMPOLY2_CUT (P2C)	P2	Define holes/openings within a MMPOLY2 boundary
MMPOLY3_CUT (P3C)	P3	Define holes/openings within a MMPOLY3 boundary
MMPOLY4_CUT (P4C)	P4	Define holes/openings within a MMPOLY4 boundary

Layer Naming

Simply associating a drawing layer with either a clear field or dark field mask can sometimes lead to ambiguous interpretations about what gets etched and what remains on the wafer. This is further complicated when multiple drawing layers are combined at the mask house to generate the actual mask. The following naming convention is being used to eliminate this confusion:

If the drawing layer name ends with the suffix "**_CUT**"
Then geometry drawn on this layer defines what gets etched away
Otherwise
Geometry defines what remains after etching

Anchor Cuts

Anchor cuts are normally intended to anchor one layer of polysilicon to the polysilicon layer immediately below it in the fabrication sequence:

X(n)C anchors P(n) to P(n-1) n=1,2,3,4

Except for P0, the SUMMiT V™ design rules do not require full enclosure of the P(n-1) layer about the X(n)C geometry. If, however, the overlap of X(n)C and P(n-1) is insufficient to form a reliable anchor or there is no overlap at all between these two layers, the condition is flagged as an "INVALID SACOXn ANCHOR".

DIMPLE Cuts

Dimple cuts are similar to anchor cuts, but they do not physically anchor to the underlying P(n-1) layers described in the previous section. The DIMPLE1_CUT is formed by a timed etch designed to stop after penetrating 1.5 μm into the 2 μm thick SACOX1, leaving a 0.5 μm clearance beneath the dimple. A timed etch is possible because the SACOX1 thickness can be well controlled. CMP processing of the SACOX3 and SACOX4 leads to thickness variations that makes pure timed approaches to creating dimple cuts less viable in these layers. Therefore, the DIMPLE3_CUT is designed to etch all the way down to MMPOLY2 much like the anchor cut is formed. Then 0.4 μm of oxide is deposited as backfill to control the dimple clearance. DIMPLE4_CUT is similarly performed, with the backfill being just 0.2 μm.

Pin Joint Cuts

Pin joint cuts are formed by first patterning MMPOLY1 with the PIN_JOINT_CUT mask. This same geometry (typically a circle) is etched into SACOX1 and undercut the MMPOLY1 to form the flange. The resulting cavity is lined with SACOX2 and backfilled with MMPOLY2.

MMPOLY1 and SACOX2 Mask Polarity

The mask that patterns MMPOLY1 is a dark field mask, whereas the other MMPOLY layers are light field. Consistent with the previously stated naming convention, the mask name associated with MMPOLY1 patterning is "**MMPOLY1_CUT**" and not MMPOLY1. Likewise, the SACOX2 mask has the opposite mask polarity from the other sacox masks. By default, MMPOLY1 remains after the MMPOLY1 etch, and SACOX2 is removed during the SACOX2 etch. Reversal of the mask polarity can be simulated by defining a boundary of MMPOLY1_CUT and by drawing a region of SACOX2 within this boundary. A MMPOLY1 structure can then be drawn as normal within a MMPOLY1_CUT region, and SACOX2_CUT can be defined within a region of SACOX2. **Note that this process is not recursive.** A MMPOLY1_CUT within a MMPOLY1 boundary that is itself contained with a MMPOLY1_CUT is not illegal, but it will not produce the desired result.

MMPOLY1 Definition

A total of 7 drawing layers together with the fabrication sequence define the actual geometry of MMPOLY1 defined here as P1''. The Boolean expression for the contribution of these layers follows:

P1C = PIN_JOINT_CUT .AND. MMPOLY1_CUT
P1' = NOT (P1C .XOR. MMPOLY1)
P2' = MMPOLY2 .XOR. MMPOLY2_CUT
X2' = SACOX2 .XOR. SACOX2_CUT
X2'' = P2' .OR. X2'
P1'' = P1' .AND. X2''

In less precise terms P1 is defined in the following way in the layout tool. Without any other layers, a polygon drawn in MMPOLY1 will not be fabricated. In the same way, a polygon drawn in SACOX2_CUT without the aid of other layers will not survive the fabrication process. A polygon drawn in MMPOLY1_CUT will be fabricated as will the intersection of MMPOLY1 and SACOX2 polygons inside it. If a SACOX2 polygon is drawn without a MMPOLY1_CUT covering it, the result is a MMPOLY1 structure.

Electrical Properties

Table 3 shows the electrical conductivity of each of the layers expressed in **Ω**/square. All polysilicon layers are n-type. The substrate is a 6-inch n-type <100> silicon wafer with resistivity of 2-20 **Ω** cm.

Table 3: ELECTRICAL CONDUCTIVITY

Layer	Mean (ohm/sq)	Std. Dev. (ohm/sq)
MMPOLY0	28.4	2.1
MMPOLY1	23.2	1.0
MMPOLY2	21.7	0.4
MMPOLY1_2	9.8	0.3
MMPOLY3	8.2	0.2
MMPOLY4	8.7	0.2

Mechanical Properties

Table 4: LAYER THICKNESS

Layer	Mean (μm)	Std. Dev. (Å)
MMPOLY0	.29	20
SACOX1	2.04	210
DIMPLE1 Depth	-	-
MMPOLY1	1.02	23
SACOX2	.3	44
MMPOLY2	1.53	34
SACOX3	1.84	5400
DIMPLE3 Backfill	.4	53
MMPOLY3	2.36	99
SACOX4	1.75	4500
DIMPLE4 Backfill	.21	30
MMPOLY4	2.29	63

Table 5: Δ W (width bias on each edge of structure)

Layer	Mean (nm)	Std. Dev. (nm)
MMPOLY1	-	-
MMPOLY2	-80	30
MMPOLY3	-70	50
MMPOLY4	-240	50

* Negative values indicate inward bias of structure resulting in actual size being smaller than drawn.

NITRIDE_CUT

A) MIN WIDTH 1.00

B) MIN SPACE 1.00

Required Layers:

Edges must be covered by MMPOLY0 & MMPOLY1

C) In most cases SACOX1_CUT should completely cover the NITRIDE_CUT with an overlap of 0.5 µm. If SACOX_1 does not cover NITRIDE_CUT completely then it must form a ring around the outside edge of the NITRIDE_CUT.
SACOX1_CUT must overlap the outside edge of the nitride cut by at least 0.5 µm and by at least 6.5 µm on the inside of the nitride cut.

Incompatible Layers:

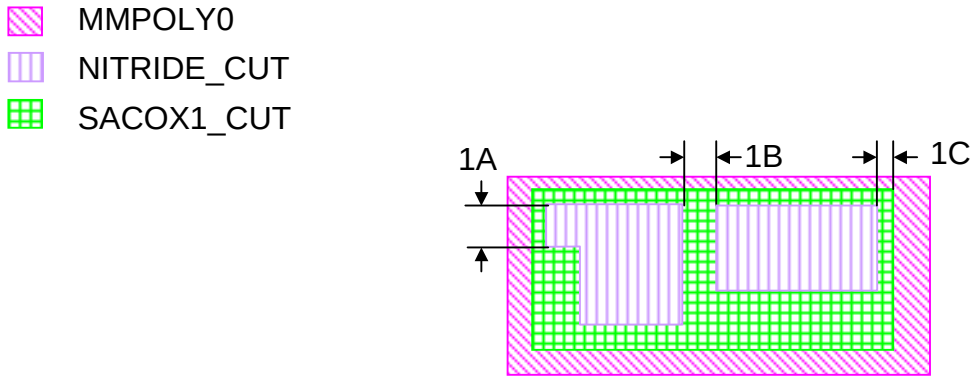
MMPOLY1_CUT about edges

Notes:

NITRIDE_CUT cuts down to the substrate removing both the nitride and oxide dielectric layers.

SACOX3_CUT may not be deep enough to anchor to MMPOLY2 in areas where it overlaps NITRIDE_CUT.

The pictures below are a graphic representation of the design rules



2) MMPOLY_0

A) MIN WIDTH 1.00

B) MIN SPACE 1.00

Required Layers:

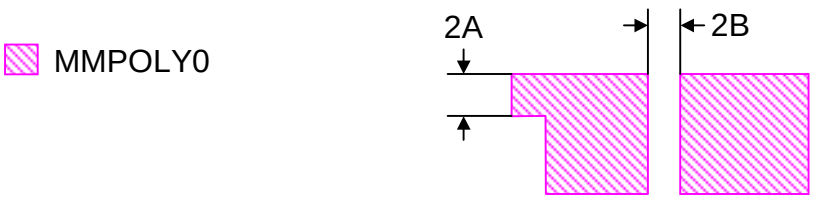
None

Incompatible Layers:

None

Notes:

A MMPOLY_0 ground plane is recommended beneath structures whenever possible.



3) DIMPLE1_CUT

A) MIN WIDTH 1.00

B) MIN SPACE 1.00

Required Layers:

C) MMPOLY1 enclosure of DIMPLE1_CUT= 0.5

Incompatible Layers:

D) SACOX1_CUT space = 1.0

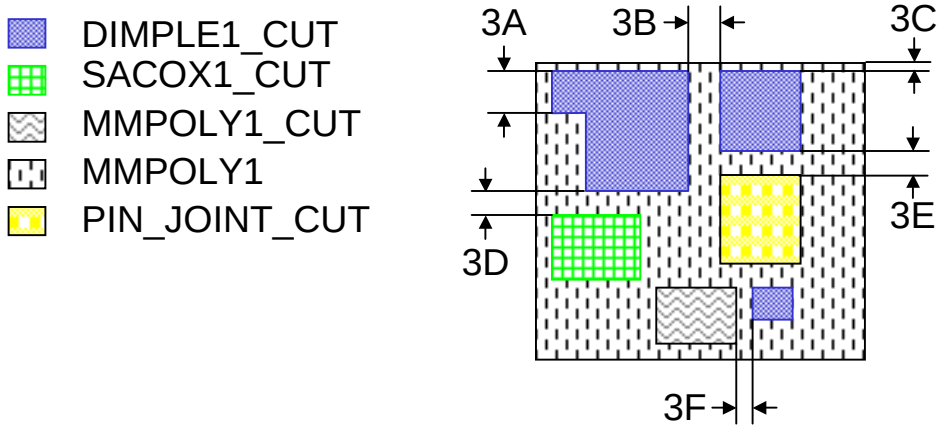
E) PIN_JOINT_CUT space = 1.0

F) MMPOLY1_CUT space = 0.5

Recommended Layers:

MMPOLY_0

Notes:



4) SACOX1_CUT

A) MIN WIDTH 1.0

with minimum area* = 3.14 μm^2

B) MIN SPACE 1.0

Required Layers:

C) MMPOLY0 enclosure of SACOX1_CUT = 0.5

D) MMPOLY1 enclosure of SACOX1_CUT = 0.5

Incompatible Layers:

E) DIMPLE1_CUT space = 1.0

F) PIN_JOINT_CUT space = 1.0

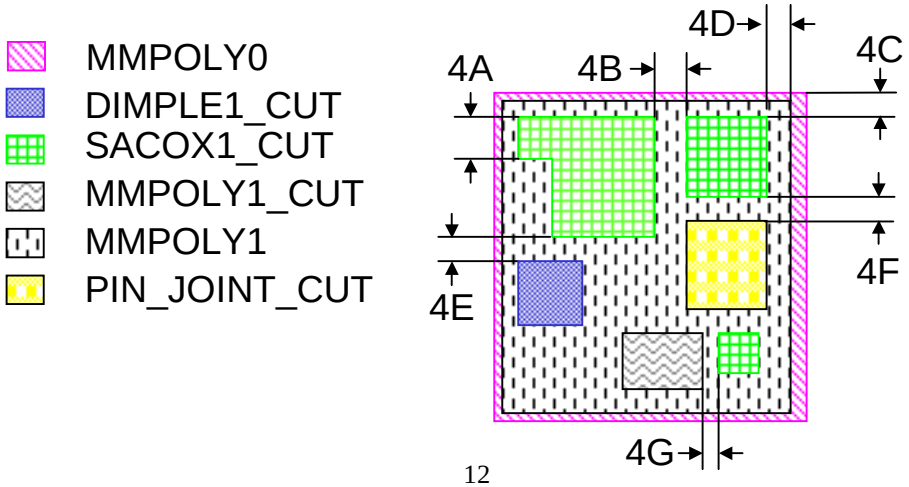
G) MMPOLY1_CUT space = 0.5

Recommended Layers:

MMPOLY_2 enclosure of SACOX1_CUT = 0.5

Notes:

*Area is based on 2-μm diameter circle, meaning that a circle this size shall fit it at least one location within the SACOX1_CUT boundary. If this is not the case, the rule is flagged as "invalid SACOX1 anchor".



5) PIN_JOINT_CUT

A) MIN WIDTH 3.0

B) MIN SPACE 7.0

Required Layers:

C) MMPOLY1 enclosure of PIN_JOINT_CUT = 1.0

D) SACOX2 enclosure of PIN_JOINT_CUT = 0.5

E) MMPOLY2 enclosure of PIN_JOINT_CUT = 1.0

Incompatible Layers:

F) DIMPLE1_CUT space = 1.0

G) SACOX1_CUT space = 1.0

H) MMPOLY1_CUT space = 1.0

I) SACOX2_CUT space = 0.5

J) MMPOLY2_CUT space =1.0

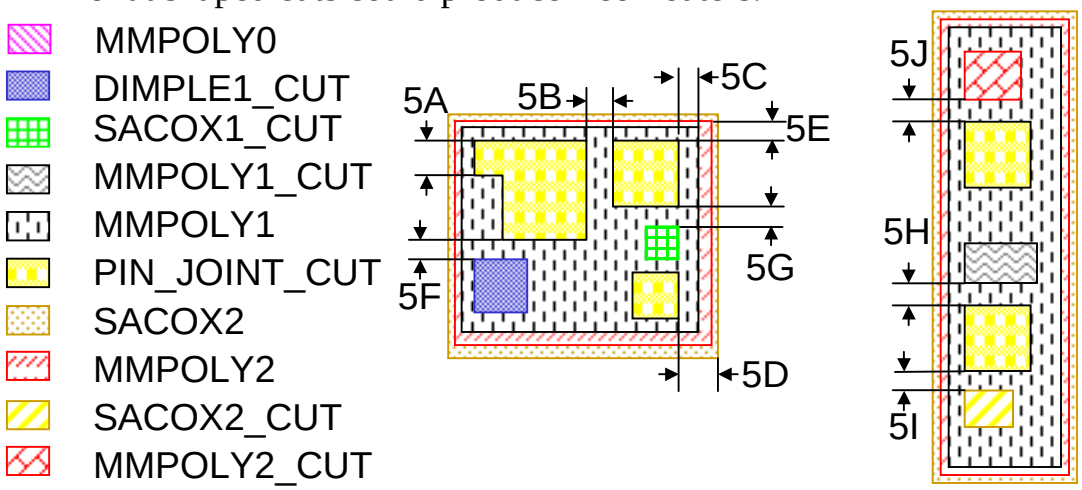
Recommended Layers:

MMPOLY0: full coverage under path of pin joint

Notes:

To operate as normally intended, adjacent PIN_JOINT_CUTs should be at least 7.0 µm apart.

Donut shaped cuts could produce free floaters.



SPECIAL RULE ABOUT MMPOLY1 ISLANDS FORMED BY PIN_JOINT_CUT

(This rule is not yet implemented in the design rules)***

A) MIN WIDTH 1.0

with minimum area* = 3.14 μm^2

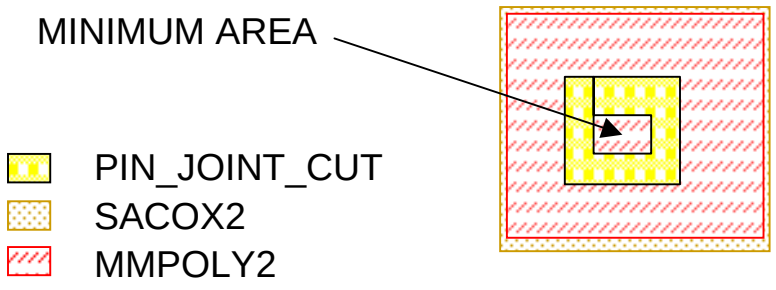
Required Layers:

Incompatible Layers:

Recommended Layers:

Notes:

Area is based on 2-µm diameter circle, meaning that a circle this size shall fit it at least one location within the MMPOLY1 island formed by the PIN_JOINT_CUT enclosure. If this is not the case, the rule is flagged as "PIN_JOINT_CUT floater".



6) MMPOLY1

A) MIN WIDTH	1.0
B) MIN SPACE	1.0

Required Layers:

MMPOLY1_CUT

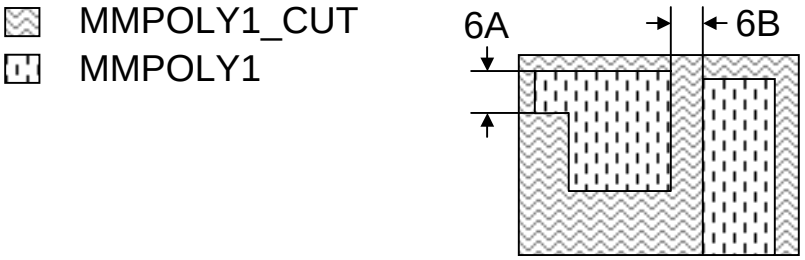
Incompatible Layers:

Recommended Layers:

MMPOLY0 under MMPOLY1

Notes:

To prevent problems due to electrostatic attenuation between polysilicon structures and the silicon nitride, MMPOLY0 is recommended under all released polysilicon structures.



7) MMPOLY1_CUT

A) MIN WIDTH 1.0

B) MIN SPACE 1.0

Required Layers:

Incompatible Layers:

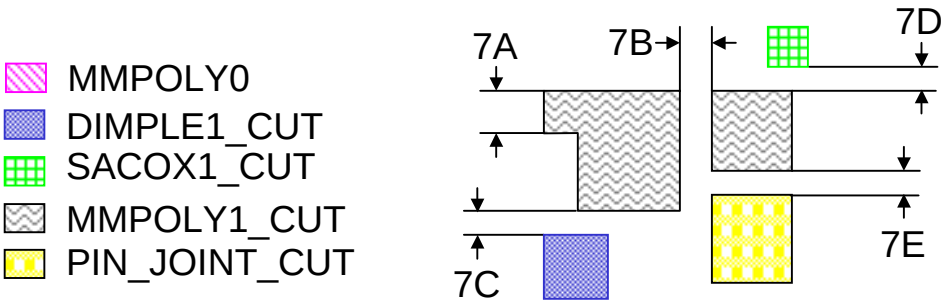
C) DIMPLE1_CUT space = 0.5

D) SACOX1_CUT space = 0.5

E) PIN_JOINT_CUT space = 1.0

Recommended Layers:

Notes:



8) SACOX2

A) MIN WIDTH 1.0

B) MIN SPACE 1.0

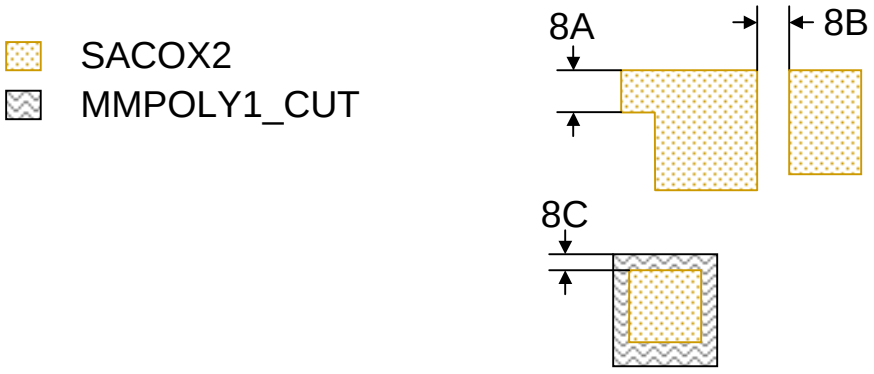
Required Layers:

Incompatible Layers:

Recommended Layers:

Notes:

C) If SACOX2 is enclosed by MMPOLY1_CUT, MMPOLY1_CUT must enclose SACOX2 by at least 0.5µm.



9) SACOX2_CUT

A) MIN WIDTH 1.0

B) MIN SPACE 1.0

Required Layers:

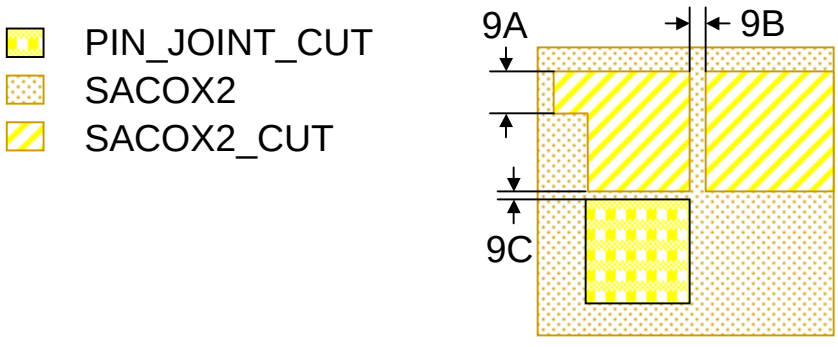
SACOX2

Incompatible Layers:

C) PIN_JOINT_CUT space = 0.5

Recommended Layers:

Notes:



10) MMPOLY2

A) MIN WIDTH 1.0

B) MIN SPACE 1.0

Required Layers:

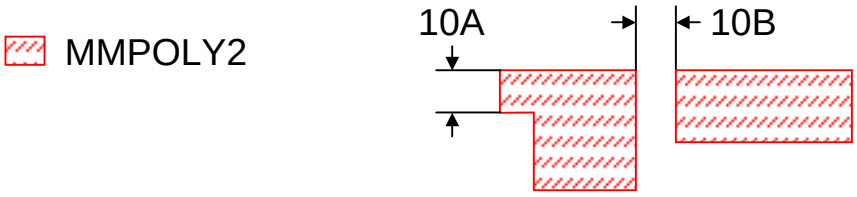
Incompatible Layers:

Recommended Layers:

MMPOLY1 (default) for mechanical rigidity

Notes:

SACOX3_CUT may not be deep enough to anchor to MMPOLY2 in areas where it overlaps NITRIDE_CUT.



11) MMPOLY2_CUT

A) MIN WIDTH 1.0

B) MIN SPACE 1.0

Required Layers:

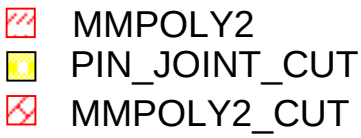
MMPOLY2

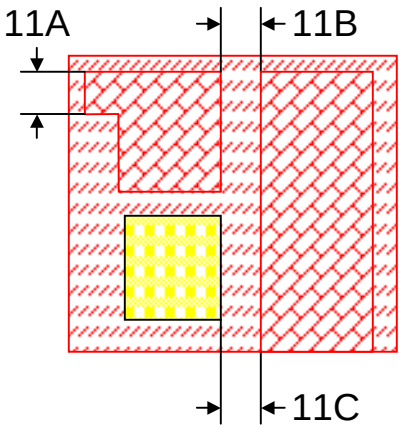
Incompatible Layers:

C) PIN_JOINT_CUT space = 1.0

Recommended Layers:

Notes:





12) DIMPLE3_CUT

A) MIN WIDTH 1.5

B) MIN SPACE 1.0

Required Layers:

C) MMPOLY3 enclosure of DIMPLE3_CUT = 0.5

Incompatible Layers:

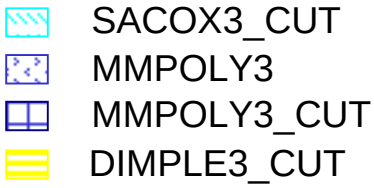
D) SACOX3_CUT space = 1.0

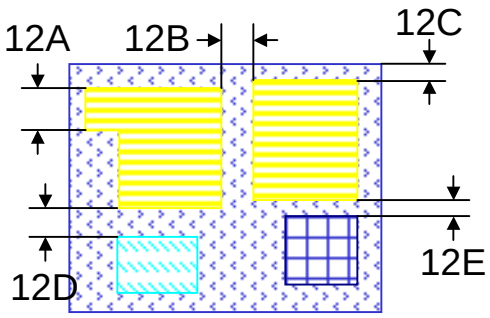
E) MMPOLY3_CUT space = 0.5

Recommended Layers:

MMPOLY2 under full DIMPLE3_CUT area

Notes:





13) SACOX3_CUT

A) MIN WIDTH 1.0

B) MIN SPACE 1.0

Required Layers:

C) MMPOLY2 (full height) minimum coincident area* = 3.14 μm^2

D) MMPOLY3 enclosure of SACOX3_CUT = 0.5

Incompatible Layers:

E) DIMPLE3_CUT space = 1.0

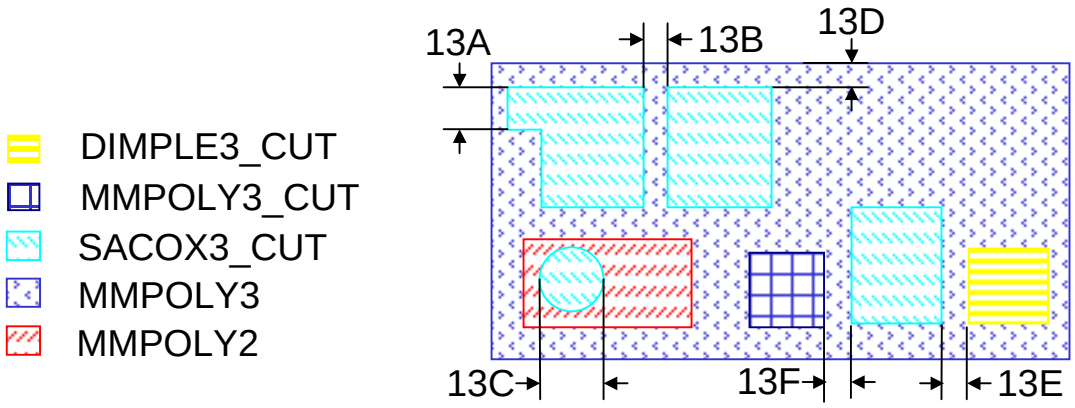
F) MMPOLY3_CUT space = 0.5

Recommended Layers:

Notes:

Depending on the design, considerable topography can be generated with underlying layers. This rule only considers the portion of MMPOLY2 that is unaffected in elevation by the removal of any of the underlying layers other than SACOX2 and MMPOLY0, although either or both can be included if desired. The result is then compared to SACOX3_CUT to ensure that a valid anchor region of at least 2 µm diameter exists. If this is not the case, the rule is flagged as "invalid SACOX3 anchor". *Coincident area is based on 2µm diameter circle.

For example, SACOX3_CUT may not be deep enough to anchor to MMPOLY2 in areas where it overlaps NITRIDE_CUT.



14) MMPOLY3

A) MIN WIDTH 1.0

B) MIN SPACE 1.0

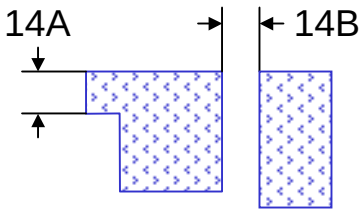
Required Layers:

Incompatible Layers:

Recommended Layers:

Notes:

MMPOLY3



15) MMPOLY3_CUT

A) MIN WIDTH 1.0

B) MIN SPACE 1.0

Required Layers:

MMPOLY3

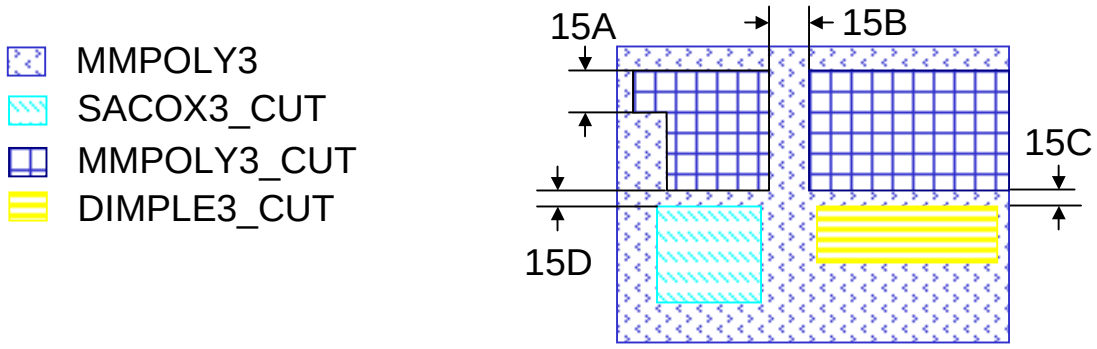
Incompatible Layers:

C) DIMPLE3_CUT space = 0.5

D) SACOX3_CUT space = 0.5

Recommended Layers:

Notes:



16) DIMPLE4_CUT

A) MIN WIDTH 1.5

B) MIN SPACE 1.0

Required Layers:

C) MMPOLY4 enclosure of DIMPLE4_CUT = 0.5

Incompatible Layers:

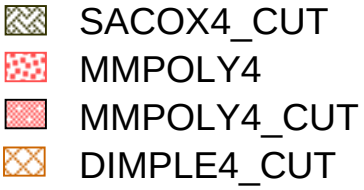
D) SACOX4_CUT space = 1.0

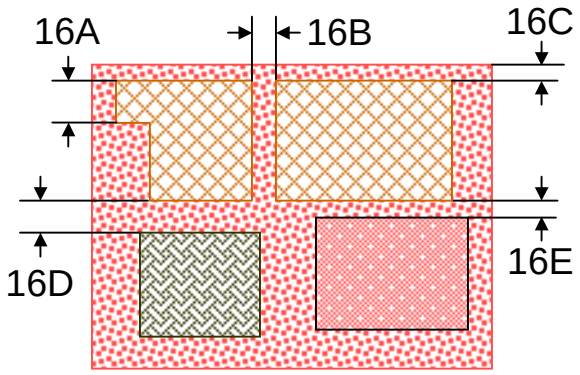
E) MMPOLY4_CUT space = 0.5

Recommended Layers:

MMPOLY3 under full DIMPLE4_CUT area

Notes:





17) SACOX4_CUT

A) MIN WIDTH 1.0

B) MIN SPACE 1.0

Required Layers:

C) MMPOLY3 (full height) minimum coincident area* = 3.14μm^2

D) MMPOLY4 enclosure of SACOX4_CUT = 0.5

Incompatible Layers:

E) DIMPLE4_CUT space = 1.0

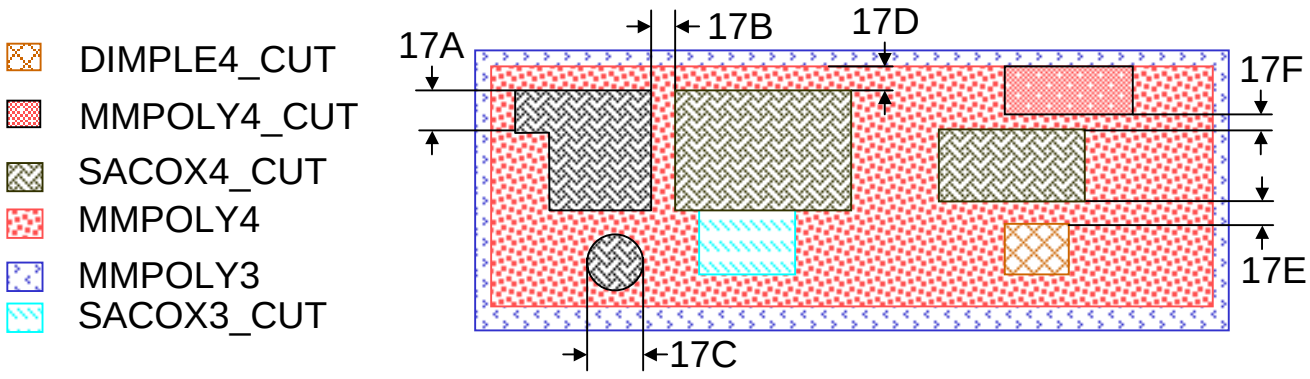
F) MMPOLY4_CUT space = 0.5

Recommended Layers:

Notes:

This rule only considers the portion of MMPOLY3 that is unaffected in elevation by the removal of any of the underlying layers. The result is then compared to SACOX3_CUT to ensure that a valid anchor region of at least 2-μm diameter exists. If this is not the case, the rule is flagged as "invalid SACOX4 anchor".

*Coincident area is based on 2-μm diameter circle.



18) MMPOLY4

A) MIN WIDTH 1.0

B) MIN SPACE 1.0

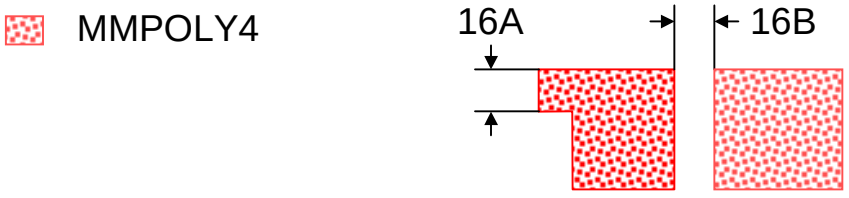
Required Layers:

Incompatible Layers:

Recommended Layers:

SACOX4_CUT

Notes:



19) MMPOLY4_CUT

A) MIN WIDTH 1.0

B) MIN SPACE 1.0

Required Layers:

MMPOLY4

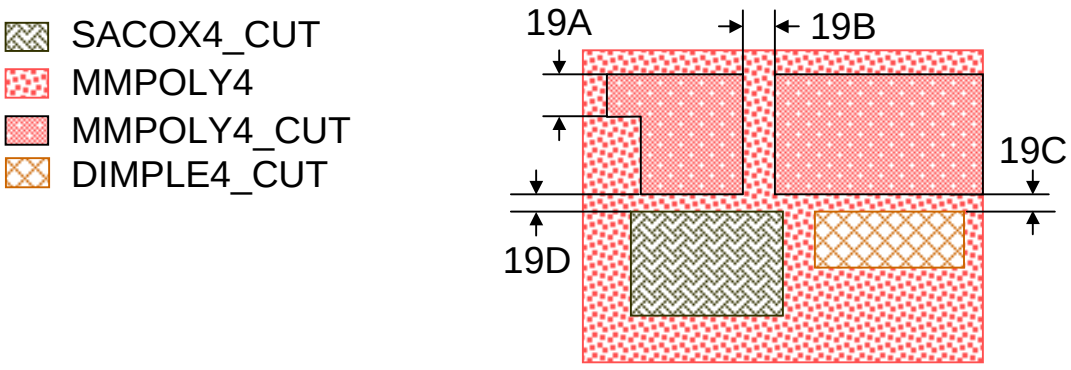
Incompatible Layers:

C) DIMPLE4_CUT space = 0.5

D) SACOX4_CUT space = 0.5

Recommended Layers:

Notes:



Summary of SUMMiT™ Design Rules

1. Minimum width and space for most layers = 1µm. The exceptions are listed below.
2. DIMPLE3_CUT and DIMPLE4_CUT: width = 1.5 µm, space = 1 µm.
3. PIN_JOINT_CUT: width = 3 µm, space = 1 µm, space for separation of PIN_JOINT_CUTs is at least 4, preferably 7 µm.
4. Minimum overlap tolerance = 0.5 µm for polysilicon and underlying cuts, MMPOLY0 + NITRIDE_CUT, MMPOLY1+DIMPLE1_CUT, MMPOLY1+SACOX1_CUT, MMPOLY3 + SACOX3_CUT, MMPOLY3 + DIMPLE3_CUT, MMPOLY4+SACOX4_CUT, MMPOLY4+DIMPLE4_CUT.

Other Design Rules and Recommendations

1. All layers must either be anchored, attached to substrate, or otherwise held down (no floating parts)
2. For many structures, the nominal dimple spacing should be every 75 µm or less. The optimal spacing is very dependent on the design of the structure and could be greater or less than 75 µm."
3. Etch release holes should be spaced 38 µm apart or closer.
4. Typical size of etch release holes is 2x2 µm.
5. MMPOLY1 and MMPOLY2 will be sandwiched and etched with the poly2 mask unless there is a SACOX2 layer surrounding the poly, i.e. a SACOX2_CUT is automatic unless specified.
6. MMPOLY1 is defined everywhere unless there is a MMPOLY1_CUT. The only way to actually draw in MMPOLY1 is to have MMPOLY1_CUT and SACOX2 surrounding it.
7. It is recommended that POLY0 be underneath all geometric features.
8. Typical size of etch release holes is 2x2 µm.
9. The following layers are required with PIN_JOINT_CUT: MMPOLY1 (1 µm enclosure), SACOX2 (0.5 µm enclosure), MMPOLY2 (2 µm enclosure). PINJOINT_CUT is incompatible with DIMPLE1_CUT, SACOX1_CUT, MMPOLY1_CUT, SACOX2_CUT, and MMPOLY2_CUT. All of the previous layers have a required space of 1 µm except for SACOX2_CUT, which has a required space of 0.5 µm.
10. Minimum area of MMPOLY1 island defined by PIN_JOINT_CUT = 3.14 µm2.
11. SACOX cuts are breakable with probes if area is less than 50µm2.
12. Although, MMPOLYX and MMPOLYX_CUT are separate layers in AutoCAD, there is only one layer of geometry produced. Except for MMPOLY1, the easiest thing is remember that cut layers are not defined where the main layer (MMPOLYX) does not exist. The purpose of the cut layer is to make it easy to draw holes (for example etch release holes) in the master layer.

Although there are exceptions, all sacox and dimple cuts should have the previously deposited polysilicon layer under them. For example, SACOX3_CUT must have MMPOLY2 underneath it. Also, the depth of dimples and sacox cuts are set assuming that there is no underlying topography. For example, a SACOX3_CUT may not contact the MMPOLY12 if the SACOX3_CUT is over a NITRIDE_CUT. A nitride cut creates a depression in the MMPOLY12. Similarly, a SACOX4 cut above a DIMPLE3_CUT may not contact the underlying MMPOLY3. Another example is a DIMPLE4_CUT that is not over MMPOLY3. Because the dimple etch does not have an etch stop, the DIMPLE4 may extend below the top surface of MMPOLY3 and cause mechanical interference. The safest course is not to have more than one cut coincident with another. The conservative size of these sacox cuts is at least 2 µm x 2 µm.

Designers should attempt to put all their designs on a 0.05 µm grid. When the masks for photolithography are created, the edges of features are snapped to this grid (including arcs and gear teeth). In addition, designers should realize that independent of the processing it is not possible to create features smaller than this on a mask plate in the standard SUMMiT™ process.